17.7 A Low-Power 2.4GHz CMOS Receiver Front-End Using BAW Resonators

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Applications for low-power, low data rate and short range wireless communications such as sensor networks require radio circuits with high-integration level and very low power consumption. Hybrid circuits combining MEMS and ICs show promising results [1-3]. This work presents an RF front-end using BAW resonators providing combined selectivity and impedance matching to a classical heterodyne receiver operating in the 2.4GHz ISM band.

Using high-Q filters with good selectivity and low insertion loss in front of a receiver relaxes the overall linearity requirements and thus, the power consumption. Moreover, heterodyne receivers need to filter out their image band in order to avoid signal degradation at the IF. Traditionally, off-chip SAW filters are used to this purpose. The feasibility of high-Q RF filters realized with BAW resonators has been demonstrated with comparable or even better results than SAW devices. An above-IC integration of a filter realized with thin film bulk acoustic wave resonators (FBAR) on top of a BiCMOS receiver front-end has been reported in [2], offering promising solutions for integration of a complete RF SoC.

The same aluminum nitride (AlN) process described in [3] but applied to solidly mounted resonators (SMR) is used. The thickness of the Al/AlN/Pt structure layers determines the resonance frequency. An additional step allows lowering it by loading the top electrode with an inert layer. In this work, the SMR devices have been integrated on a separate substrate. Test resonators having a coupling factor k^2_{eff} of 5.6% and series resonance Q as high as 580 were measured.

The block diagram of Fig. 17.7.1 describes the architecture of the heterodyne front-end. The BAW filter is placed in front of the LNA to eliminate out-of-band interferers and relax the linearity requirements. A Gilbert switching mixer follows the LNA and downconverts the RF signal to the 100MHz IF. For measurement purposes, the front-end is terminated by source-follower output buffers.

RF filters need correct impedance terminations in order to perform as specified. Input impedance matching is therefore a critical part of the LNA design. Classical LNAs require several critical inductors [4] to provide a real input impedance (typically 50Ω). On-chip inductors require a large silicon area and only offer limited quality factor. The main novelty of this work is to co-design the LNA and the filter using BAW resonators. With this approach, the input impedance matching is inherently accounted for and the designer can take advantage of extra degrees of freedom in sizing the resonators. Moreover, the use of only high-Q passive components helps in achieving better gain and noise figure performance.

The proposed selective LNA topology is shown in Fig. 17.7.2. Similar to lattice filters, the Y_1 and Y_2 resonators are appropriately detuned to achieve the widest bandwidth. These devices are mutually coupled through the network formed by the transistors and the cross-coupled capacitors. As shown in Fig. 17.7.3, the resulting gain of the selective LNA shows a bandpass characteristic. A fully differential topology is chosen for better immunity to substrate and power supply noise. Moreover, balanced operation is mandatory for lattice filters and similar circuits such as the presented selective LNA. In order to improve the out-of-band rejection, a prefilter stage is added in-front of the circuit. This prefilter is a lattice network built from identical resonators with those used in the selective LNA. Hence, the total number of resonators amounts to 8 and the implementation requires only one loading step. The main transistors are cascoded to improve reverse isolation and stability. The amplifier is loaded by an LC tank, the quality factor of which determines the output impedance and gain of the amplifier. The tank inductor is a differential integrated inductor using the 5 upper metal layers of the digital CMOS process. In order to realize a trimming capability on the load resonance frequency, several switched capacitors are added in parallel to the output nodes. If a smaller gain is acceptable, the LNA output current could be directly connected to the downconversion mixer, leading to an inductorless design.

To measure the circuit, both chips were bonded together and to external I/Os directly on a PCB as shown in Fig. 17.7.7. In order to convert the single 50Ω generator output into a 100Ω differential input to the circuit, an external passive balun is used, resulting in slight degradation of the overall noise figure due to its insertion loss (~0.8dB for the chosen component). The RF selectivity is measured with a constant IF frequency (90MHz) and the results are shown in Fig. 17.7.3. It can be seen that measurements are close to the simulated results, with a center frequency shifted upwards by ~80MHz. This is due to a thinner piezo-electric layer than expected. Though this effect can be compensated for with a loading layer on the resonators, it requires an additional step which was not included for this prototype. The overall voltage gain of 12dB is 6dB lower than simulation and the noise figure is degraded accordingly. This is mainly due a lower Q than expected for the LC load and probably to an additional problem with the external balun interconnects. The measured noise figure for the overall front-end amounts to 11dB. While this value seems unduly high, it has to be noted that it includes all insertion losses in the balun and the filter, as well as the mixer noise in some proportion depending on the LNA gain. The impedance matching at the balun input is measured with a vector network analyzer and the input reflection coefficient is as low as -10dB in the passband (Fig. 17.7.4) without any external matching network. The bump in S_{11} at mid-band is due to an inaccurate detuning of the resonators. This is also the cause of the mid-band ripple on the gain curve. Figure 17.7.5 shows the results of a dual-tone linearity measurement and the measured results are summarized in Fig. 17.7.6.

A low-power Rx heterodyne front-end is presented that shows high selectivity and good image rejection. The LNA uses coupled high-Q BAW resonators to provide both input impedance matching and selectivity, as well as low-power consumption. Hence, it offers a good alternative to other impedance matching schemes.

Acknowledgments:
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[2] J.F. Carpentier et al., "A SiGe:C BiCMOS WCDMA Zero-IF RF Front-End using an Above-IC BAW Filter," *ISSCC Dig. Tech. Papers*, pp. 394-395, Feb., 2005.
[3] M.-A. Dubois et al., "Integration of High-Q BAW Resonators and Filters Above IC," *ISSCC Dig. Tech. Papers*, pp. 392-393, Feb., 2005.
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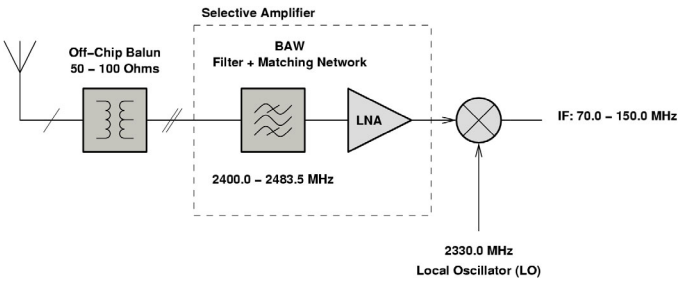

Figure 17.7.1: Heterodyne front-end architecture.

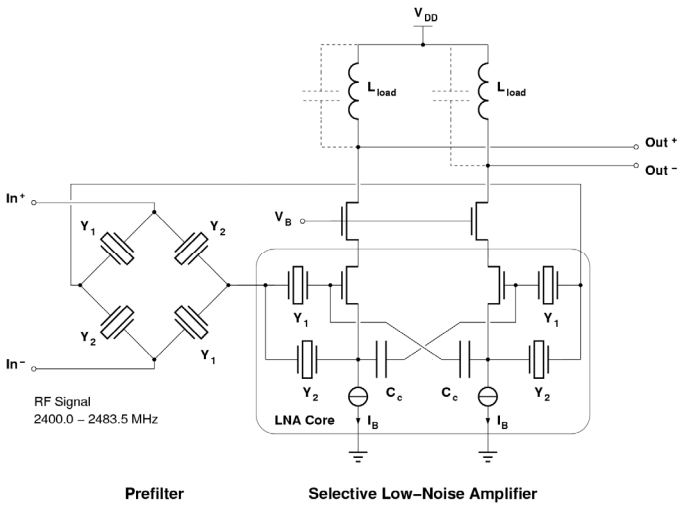

Figure 17.7.2: Selective low-noise amplifier schematic.

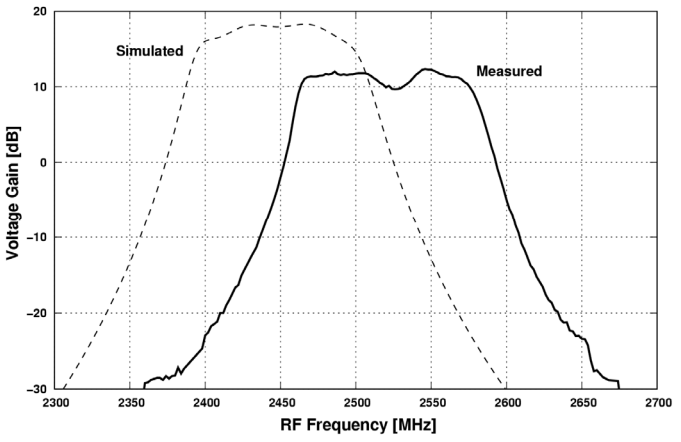

Figure 17.7.3: RF front-end selectivity.

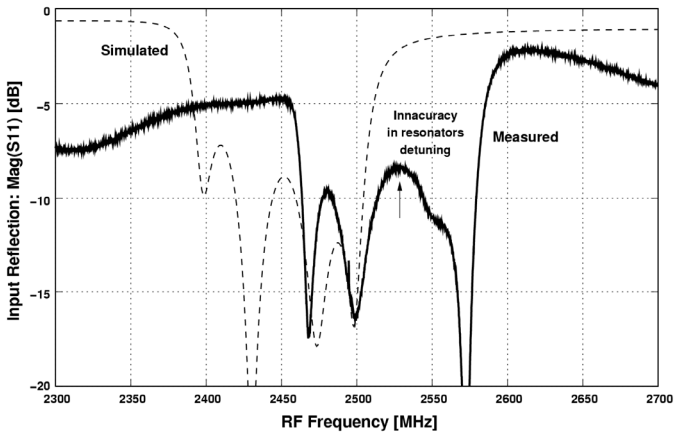

Figure 17.7.4: Magnitude of the input reflection coefficient.

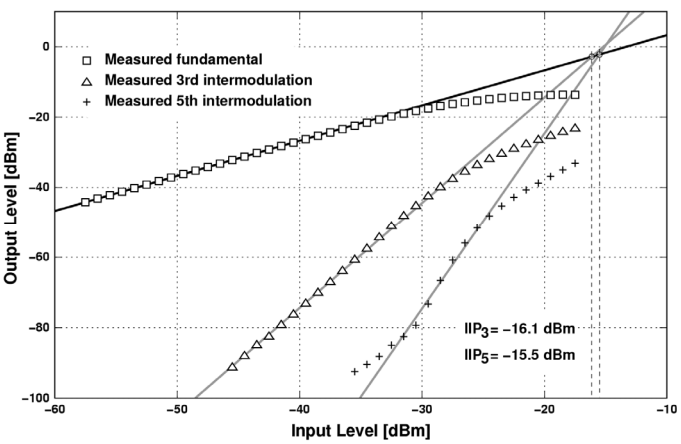

Figure 17.7.5: Dual-tone measurement of the front-end linearity.

Measurement made at T = 25°C, f_{RF} = 2.5GHz, f_{LO} = 2.41GHz			
Parameter	Condition		Units
Supply voltage		1.2	V
Current consumption	including bias, w/o output buffers	1.5	mA
Power consumption		1.8	mW
Voltage gain		12	dB
Image rejection		50	dB
RF bandwidth		100	MHz
Noise figure		11	dB
Input 1dB compression		-26	dBm
Input IP_3	2499.5MHz, 2500.5MHz	-16.1	dBm

Figure 17.7.6: Front-end measured results summary.

Continued on Page 656

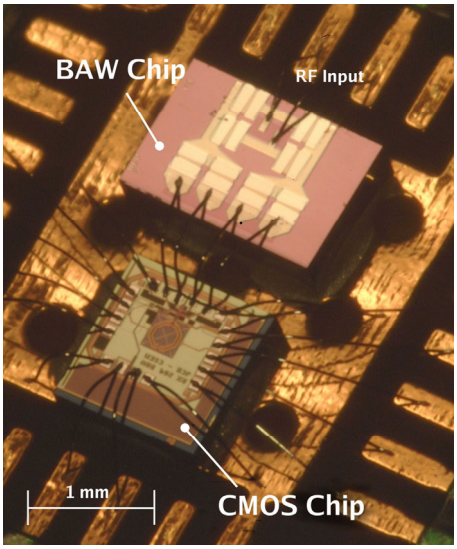

Figure 17.7.7: Micrograph of the two chips bonded together and on PCB.

